The Dependence of Electrical Characterization on Interface Structure of PtSi/strained-Si$_{1-x}$Ge$_x$/Si Schottky Diodes

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Abstract:
PtSi/strained Si$_{1-x}$Ge$_x$ (x = 0, 0.2 and 0.25) Schottky barrier diodes (SBD) with extended cutoff wavelengths have been demonstrated using by combining pulsed laser deposition (PLD) and molecular beam epitaxy (MBE). Pt was deposited by PLD on the Si$_{1-x}$Ge$_x$ alloys with a thin Si sacrificial cap layer fabricated by MBE. By the reaction of deposited Pt film on Si sacrificial cap layer silicide SBD have been fabricated. Auger electron depth profiling was performed on the films before and after in vacuo annealing to study the redistribution of composition in the reactions. High-resolution transmission electron microscopy (HREM) was used to investigate the interface structure. We have found that Pt react mainly with Si to form silicides at 350°C, leaving some Ge to segregate at the surface. While, with the annealing at 600 °C for 3min the interface of PtSi/Si$_{1-x}$Ge$_x$ is smooth, and its electrical characterization is prior. Since lowered-barrier-height silicide SBD are desirable for obtaining longer cutoff-wave-length Si-based infrared detectors, the Schottky barrier heights (SBH) of the PtSi/strained Si$_{1-x}$Ge$_x$ SBDs with smooth interfaces were substantially lower than those of PtSi/Si SBDs, i.e. decreased with increasing Ge fraction, allowing for tuning of the SBDs cutoff wavelength. The SBH of PtSi/Si$_{1-x}$Ge$_x$/Si has been found to vary between 0.12-0.58 eV in the temperature range 77-293 K. At 293 K, the ideality factor has been found to be 2.00 and 1.32 for PtSi/Si$_{0.80}$Ge$_{0.20}$ and PtSi/Si$_{0.75}$Ge$_{0.25}$ diodes, respectively. We have shown that high quantum efficiency and near-ideal dark current can be obtained in the film of PtSi/strained Si$_{1-x}$Ge$_x$ with excellent interface fabricated by MBE and PLD, furthermore annealing at 600°C for 3min.

Keywords:
Schottky barrier heights (SBH); HREM; Strained Si$_{1-x}$Ge$_x$ layers; Interface structure
Introduction

Since the concept of silicide Schottky-barrier detector (SBD) focal plane arrays (FPA’s) was proposed by Shepherd and Yang in 1973[1], the silicide/Si FPA has become the most mature technology for large-area, high-density FPA’s for many short-wavelength infrared (SWIR, 1 to 3 µm ) and middle-wavelength infrared (MWIR, 3 to 5 µm ) applications. This is due primarily to that the infrared imagers are fabricated by well-established silicon VLSI processes[2-4]. Since the strained Si$_{1-x}$Ge$_x$ on Si (100) has a smaller bandgap than silicon, with most of the band offset in the valence band, thus, the Schottky-Mott model of metal-semiconductor contacts predicts that a silicide/strained Si$_{1-x}$Ge$_x$ diode will have a lower p-type Schottky-barrier height than the corresponding silicide/Si SBD. Hence one can expect a longer cutoff wavelength from a silicide-strained Si$_{1-x}$Ge$_x$ Schottky diode. While the extended cutoff wavelengths has been the motivation for silicide/SiGe detectors, another useful effect, that of highly voltage-variable barrier heights, and be obtained by using the SiGe/Si valence band offset in conjunction with the PtSi/SiGe Schottky barrier.

The electrical properties of a practical SBD are mainly controlled by the interface properties and a study of the interface quality is important. It is well established that PtSi/Si contacts can be prepared by thermally reacting Pt with Si to form a PtSi[5]. The formation of abrupt, near-ideal silicide/SiGe interfaces is not as simple as the formation of comparable silicide/Si interfaces, because of the more complex chemistry of metal-SiGe reactions. Many reports dealing with the thermal reaction of Pt with strained Si$_{1-x}$Ge$_x$ have shown that it is difficult to fabricate a well-defined, reproducible PtSi/Si$_{1-x}$Ge$_x$ junction using this technique[6-7]. This is due to the fact that both the segregation of Ge to the surface and/or Ge pile-up at the junction results in uncontrolled chemical structure at the silicide/Si$_{1-x}$Ge$_x$ interface. An approach to avoid this problem is to grow a thin Si cap layer on the strained Si$_{1-x}$Ge$_x$ epitaxial layer to be consumed during the silicidation process, forming an abrupt metal-silicide- Si$_{1-x}$Ge$_x$ junction[8]. There have been conflicting reports on the SBH of PtSi/Si$_{1-x}$Ge$_x$ junctions produced by the thermal reaction, reflecting the complicated nature of this structure.

In this article, we present the results on the fabrication and electrical characterizations of PtSi/Si$_{1-x}$Ge$_x$ Schottky diode structures comparing with PtSi/Si diode. The thickness of the GeSi alloys is dictated by the critical thickness limit beyond which pseudomorphic growth is no longer warranted.

Experimental procedure

The strained p-Si$_{1-x}$Ge$_x$ samples used in this study were grown by MBE (V80 MBE system) on lightly doped p-type Si (100) oriented substrate at 750°C. The base pressure in the growth chamber was $4 \times 10^{-10}$ Torr. An elementary boron source was used to dope the grown strained Si$_{1-x}$Ge$_x$ to a doping level of approximately
3×10^{19} \text{cm}^{-3}$. P-type Si (100) CZ wafers with a resistivity of 8-13 $\Omega \cdot \text{cm}$ were used as substrates and their temperature was controlled by an optical pyrometer. Prior to loading in the ultrahigh vacuum (UHV) sputtering chamber, the surface was subjected to an ex situ chemical cleaning procedure (a modified RCA method, described elsewhere\cite{9}). Then the substrates were slowly annealed up to 450°C taking care to maintain the pressure below 6.8×10^{-8} \text{Torr}. This treatment was followed by flash heating at 880°C allowing desorption of the thin oxide film. After the deposition of a 100nm Si buffer layer at 750°C, the nominal Si$_{1-x}$Ge$_x$ ($x = 0.2$ and 0.25) layers were deposited on top of these buffer layer, capped with a Si sacrificial layer designed to be consumed during the silicide formation of the Schottky diode fabrication. The Si cap layers also ensure alloy passivation against air exposure contamination during transport from the preparation chamber to different units.

After a high-quality protective oxide layer was formed and windows were opened in the oxide, silicide was selectively formed inside these windows using PLD and laser annealing processes. The sacrificial layer was 4 nm, and the metal was 2.5 nm, these thicknesses were chosen so that the silicon sacrificial cap layer would be exactly consumed in the silicide formation process. This process ensures a Schottky contact with a pure silicide film (without Ge), at the same time, eliminates the Ge segregation at the interface that could cause Fermi level pinning.

The diodes were processed in a clean room environment. Si$_{1-x}$Ge$_x$/Si samples were cleaned in acetone, methanol, and de-ionized (DI) water consecutively. Before loading into the UHV chamber for Pt deposition, samples were hydrogen terminated by dipping in a dilute HF solution (1-2%) for 2 min to remove the native oxides, which slightly reduces the Si cap thickness and was accounted for in selecting the metal layer thickness. The Pt depositions were done by PLD in a load-locked UHV system. The base pressure of the chamber was 2×10^{-9} \text{Torr} by employing a liquid nitrogen-cooled titanium sublimation pump. Other growth conditions and a detailed description can be found in Ref. 10. After standard cleaning the surface was hydrogen terminated by dipping in diluted HF. Aluminum was then evaporated onto some parts of the front side of the samples to form ohmic contacts. This was followed by a 450°C sintering under pure Ar atmosphere.

The interfacial reaction of Pt with Si$_{1-x}$Ge$_x$ was studied by the Auger depth profile before and after in vacuo annealing. SBH were inferred from the saturation current obtained in the forward current-voltage characteristics measured at room temperature and 77K. The effective Richardson constant for Si$_{1-x}$Ge$_x$ is taken as the sum of the weighted value of pure Si (112 A/cm$^2$K$^2$) and Ge (50 A/cm$^2$K$^2$)\cite{11}. The film thickness and its uniformity were examined using high resolution TEM (HREM).

**Result and discussion**

1. **Interfacial reaction of Pt on epitaxial Si$_{1-x}$Ge$_x$ alloys**

From the Auger depth profile (Fig.1), it is clearly seen that Ge was incorporated into
the reacted layer after annealing. After the annealing at 600°C for 3 min, the entire Pt film was consumed, and the spreading of the Si as so as Ge profile with a higher Ge concentration at the surface were observed as shown in Fig. 1 (b). The higher Ge concentration at the reacted film surface indicates a surface segregation of Ge. HRXRD analysis showed the reflections of Pt(Si₁₋ₓGeₓ) and PtGe₂ after 30 min annealing at 350°C. It cannot be resolved by XRD analysis, whether the Pt (Si₁₋ₓGeₓ) compound is ternary or a mixture of PtSi and PtGe[11]. The AES result shows that Ge reacts with Pt to some degree, which cannot found from the XPS study. All of the experimental results strongly indicated that the reaction at 600°C between Pt and Si₁₋ₓGeₓ consists of the inter-diffusion of Pt, Si and Ge. In the process of the reaction Pt is the dominant diffusion species, meanwhile Pt diffuses in and some Ge diffuse out. According to the thermodynamic data[12], it is known that Si is more reactive than Ge with Pt. As Pt atoms reach the silicide/ Si₁₋ₓGeₓ interface, they react preferentially with Si to form a silicide, and then the Ge atoms, which are left behind, diffuse out and pile up at the surface.

Another series of separate experiments with different annealing temperatures show that the surface Ge concentration increases with annealing temperature. The higher the temperature, the greater the difference in reaction rate, it means that the lesser the chance for Ge to react with Pt. In addition, the diffusion constant increases with temperature, as does the surface Ge concentration.

2. Interface structure studied by HRTEM

A cross-section micrograph has been made by HREM. The sample is first cut into two pieces, which are then glued together with the grown layers face to face. After that, the cross-section is mechanically thinned to a thickness of about 80μm, followed by dimpling to a thickness of about 10μm. The dimpled sample is finally ion milled to electron transparent, and then observed in a field emission 300 kV Philips CM 300 TEM. Fig. 2 shows the cross-sectional crystal lattice images of HREM for annealing at 600°C for 3 min. The film thickness of GeₓSi₁₋ₓ layer is approximately 2 nm, and the thickness of PtSi layer is about 3 nm on this formation conditions. To know more about the continuity and uniformity of the films, the large area HREM crystal lattice images of sample were developed. It is seen that the films of GeₓSi₁₋ₓ layer and PtSi layer are continuous and uniform. Also, the roughness of the layer remains the same. Analysis of the surface roughness with atomic force microscope (AFM) showed an average roughness of 3.3 nm over a 0.5×0.5 μm² area.

3. Electrical properties of PtSi/Si₁₋ₓGeₓ and PtSi/Si diodes

As the photodetection mechanism of a silicide SBD is based on the photoemission of holes from the silicide to the semiconductor, the cutoff wavelength is determined by the SBH. If the effect of the surface states is neglected, the barrier height Φₘₛ of the metal/p-type semiconductor is given by[13]:

\[ q\Phi_{ms} = q\chi_s + E_g - q\Phi_m \]
where $\chi_s$ and $E_g$ are the electron affinity and bandgap of the semiconductor respectively and $\Phi_m$ is the work function of the Pt metal. Strained Si$_{1-x}$Ge$_x$ on Si (100) has a smaller band-gap than silicon, with most of the band offset in the valence band, and also the electron affinity may be assumed to be the same as that of Si\textsuperscript{[14]}. The current-voltage characteristics of an ideal SBD are given by

$$I = I_0 [\exp(qV/kT) - 1]$$

Where $I_0$ is the saturation current, i.e. the current at zero applied bias. $V$ is the applied voltage across the diode. $q$ is the electronic charge. $k$ is the Boltzmann constant, and $T$ is the absolute temperature. Considering non-idealities at the metal-semiconductor contact, the I-V characteristics of a SBD can be expressed as

$$I = I_0 [\exp(\frac{q(V - IR)}{nkT}) - 1]$$

and

$$I_0 = A\bar{A}T^2 \exp(-q\Phi_m kT)$$

Where $R$ is the series resistance usually present in the device. $A$ is the device area, $A^*$ is the effective Richardson's constant, $\Phi_m$ is the zero-bias barrier height, and $n$ is the ideality factor. Assuming that thermionic emission is the main mechanism for current flow in the structure, the barrier height was calculated using the relation

$$\Phi_m = (kt/q) \ln(A\bar{A}T^2 / I_0).$$

The forward logarithmic I-V characteristics of different diodes are shown in Fig. 3 (a: PtSi/Si), (b: PtSi/strained Si$_{0.75}$Ge$_{0.25}$) and (c: PtSi/strained Si$_{0.8}$Ge$_{0.2}$) at temperature of 77K, 150K and 293K respectively. The saturation current, i.e. the current at zero applied bias of a Schottky diode, is usually obtained by graphically extrapolating the linear portion of the forward I-V characteristics to zero applied bias. With the help of this saturation current the important parameters for the Schottky diode (barrier height, ideality factor) can be calculated. However, the above method is difficult to apply at large bias voltage where the voltage drop across any possible series resistance may become a significant proportion of the applied voltage. To avoid this difficulty the saturation current and ideality factor can be calculated by using a least squares fitting method\textsuperscript{[15]}. Table 1 shows the dependence of the barrier height on temperature. It is seen that the SBH increases with increasing temperature in the temperature range considered here. The temperature dependence of the barrier height is due to the fact that for SBD the measured current is a combination of the thermionic current and the recombination current. As a result, the barrier height values calculated using the thermionic emission model show temperature dependence, since the deviation from ideal behavior due to
that the recombination becomes more prominent as the temperature is lowered. In addition, the presence of a native oxide on the strained Si$_{1-x}$Ge$_x$ layer strongly influences the temperature dependence of the barrier height.

The temperature dependence of the barrier height of a PtSi/p-Si Schottky diode processed in the same run has also been shown for comparison purposes. At a particular temperature, the barrier heights of PtSi/Si$_{0.8}$Ge$_{0.2}$ and PtSi/Si$_{0.75}$Ge$_{0.25}$ SBD are smaller than that of a PtSi/p-type Si Schottky diode. The biaxial strain in Si causes a change in the bandgap, and is empirically given by

$$E_g(x) = 1.12 - 0.74x \text{ eV}$$

Where $x$ is the Ge concentration. Hence the band-gap reduction is 0.13 eV for the 20% Ge concentration and is 0.20 eV for the 25% Ge concentration. This band gap reduction is the reason for the smaller barrier height obtained for PtSi/strained Si$_{1-x}$Ge$_x$ Schottky diode. From Table 1, we see that the reduction of barrier height for the PtSi/strained Si$_{1-x}$Ge$_x$ is not the same as is expected from the theoretical predictions due to the reduced bandgap. But it is also evident that the SBHs of the PtSi/Strained Si$_{1-x}$Ge$_x$ Schottky diode decrease with the increase in Ge mole fraction.

The value of the ideality factor, calculated from the experimental I-V characteristics at room temperature are found to be 2.0, 2.0 and 1.32 for PtSi/p-Si, PtSi/Si$_{0.8}$Ge$_{0.2}$ and PtSi/Si$_{0.75}$Ge$_{0.25}$, respectively. The I-V characteristics are especially dependent on the interface quality. In a Schottky diode, even with a good surface treatment, an interfacial oxide layer of thickness about 0.5 to 1 nm with a considerable density of surface states is expected. According to the Bardeen model these surface states can pin the Fermi level at the midgap of the energy band and make the SBH less sensitive to the metal work function. The departure of the ideality factor from unity may due to the interfacial layer between the metal and the semiconductor. Another reason may be the existence of a laterally varying potential barrier height, caused by a nonuniform interface. And the nonidealities are mostly due to the states associated with the defects near the surface of the semiconductor. These defects act as recombination centers giving rise to excess current that causes deviation from the ideal thermionic emission behavior at low voltage and low temperature. In addition, image force lowering and thermionic field emission result in a deviation of the ideality factor from unity. In the present structure, several interfaces are also involved and may be contributing to a higher value of the ideality factor. The effects of heterointerfaces become more prominent at lower temperature, thus the ideality factor increases.

**Conclusion**

MBE has been employed for the epitaxial growth of strained Si$_{1-x}$Ge$_x$ layer. PtSi/strained Si$_{1-x}$Ge$_x$ SBDs have been fabricated on these strained layers, where the silicide was produced by PLD. It can be seen that, after the annealing at 600°C for 3 min, the Pt reacts with Si, and PtSi forms based on Si$_{1-x}$Ge$_x$/Si, since a little surface segregation of Ge occurs.

In summary, HREM study shows that the film thickness of Ge$_x$Si$_{1-x}$ ($x = 0.2$ and 0.25) layer is approximately 2 nm, and the thickness of PtSi layer is about 3 nm of the
sample annealed at 600°C for 3 min. It can be seen that the films of Ge$_x$Si$_{1-x}$ layer and PtSi layer are continuous and uniform. Meanwhile, analysis of the surface roughness showed an average roughness of 3.3 nm over a 0.5×0.5 µm$^2$ area.

In addition, these are the first electrical results from PtSi/Si$_{1-x}$Gex diodes produced with this technique. The SBH with Ge fraction $x$ was found to decrease almost the same as the bandgap of strained Si$_{1-x}$Gex. The variations of barrier height and ideality factor have been studied as a function of temperature. The cutoff wavelength is tunable by the amount of Ge, cutoff wavelength over 8 µm has been obtained, and extension to 10 µm should be straightforward. It was then suggested that PtSi/Si$_{1-x}$Gex diodes could be employed in the infrared detector applications with the possibility of tuning the cutoff wavelength.

REFERENCES
Fig. 1 Auger depth profiles of the PtSi/Ge$_{0.2}$Si$_{0.8}$/Si.
(a) Pt/Ge$_{0.2}$Si$_{0.8}$/p-Si without annealing, (b) Pt/Ge$_{0.2}$Si$_{0.8}$/p-Si annealed
Fig. 2 HREM image of PtSi/Ge$_{0.2}$Si$_{0.8}$/p-Si sample. Film surface and interface are indicated by arrows.
Fig. 3 Forward and reverse I-V characteristics at different temperatures for
(a) PtSi/p-Si Schottky diodes, (b) PtSi/Ge_{0.25}Si_{0.75} Schottky diodes
| Temperature /K | | | | | | | |
|----------------|----------------|----------------|----------------|
| 77      | 0.12 | 0.13 | 0.19 | | | | |
| 150     | 0.28 | 0.31 | 0.32 | | | | |
| 293     | 0.52 | 0.57 | 0.58 | | | | |
| Ideality factors (293K) | 1.32 | 2.0 | 2.0 | | | | |

Table 1 Comparisons of the barrier height and ideality factor of PtSi/Ge$_x$Si$_{1-x}$/Si and PtSi/p-Si